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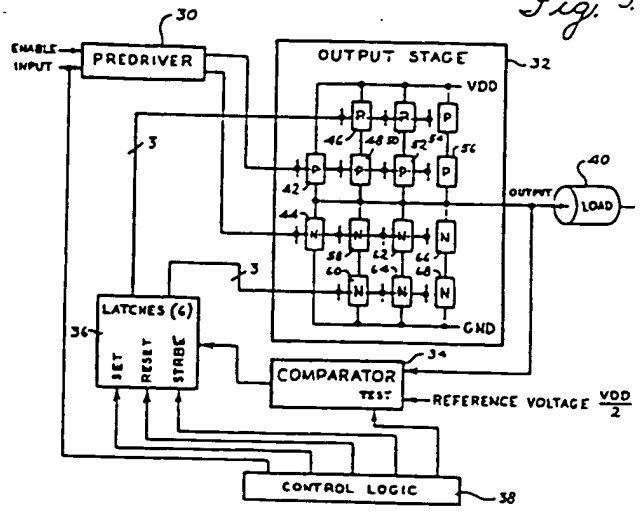
(54) Self-adjusting impedance matching driver.

(57) A self-adjusting impedance matching driver for a digital circuit. The driver has both a pull-up gate (42) to VDD and a pull-down gate (44) to ground. An array of gates is provided in parallel with each of the pull-up gate and the pull-down gate, with any one or more of such gates being selectively enabled in response to circuit means that monitors the impedance match between the output of the driver and the network it drives. By enabling selectively such gates, any impedance mismatch can be minimized. The selective enablement may be done only at power up, and thereafter only if the driven network is changed substantially.

Fig. 3.



EP 0 463 316 A1

son is made. All incremental impedanc pairs are initially on. In any such test, if the result of the comparison is, in the case of th p-typ d vices, that the utput voltage is more than the r fer nce voltage (less, in the case of the n-type devices), additional gate pairs are incrementally gated ff subtracting impedance in parallel with the impedance with the primary output driver devices 42, 44. Wh n the result of the comparison is the opposite, additional gate pairs are left on.

The impedances associated with the respective incremental impedance pairs are not all the same. Rather, they are provided in values spanning roughly continuously across a range, from highest to lowest, representing, in a sense, the least significant bit to most significant bit of incremental impedance contribution. According to one embodiment, a successive approximation algorithm is utilized to determine which pairs of gates are enabled to adjust the impedance to its optimum value. Rather than simply turning on the gate pair representing the highest impedance, and then continuing successively to that having the smallest resistance, or vice versa, all gate pairs are initially turned on. The gate pair having the smallest impedance, representing the most significant bit, is then turned off first, setting the overall impedance in the midrange of the entire range. This divides the range of all possible impedance values for the output stage 32 into two sections: High and Low. The test is then conducted, which determines whether to go higher or lower in impedance, i.e., whether this most significant bit of incremental impedance is to remain off, or be turned back on. According to successive approximation, after making this first impedance adjustment, the range of potentially optimal resistances is divided again into two sections as before by turning off the next less significant bit of incremental impedance, the test is made, and so forth.

In an arrangement such as that shown in Figure 3, wherein three additional incremental impedances are provided, the impedance should approximately, and optimally for this configuration, match the load impedance after the third iteration of this successive approximation algorithm. This impedance matching scheme can match up to eight different resistances by sending out just three pulses (the pull-up portion is matched on the rising transitions and the pull-down portion is matched on the falling transitions).

Typical impedance values in conventional digital circuitry requiring I/O drivers range from 20 to 100 ohms. Using this range in the preferred embodiment allows the designer to use this driver in almost all situations without having to worry about the impedance. As mentioned above, with three bits there are eight different r sistances.

How ver, the weighting of the incr mental impedance values determines th spr ad f the resistances. The pr ferred emb diment was d v loped for use in a d sign system that pr viously provided impedanc s of 20, 40, and 80 ohms. Consequently, an attempt was made to provide these specific values. However, practical considerations lead to the dropping of the 20 ohm value. Since process variations change the resistances of the MOS devices utilized, the highest impedance should be set around 100 ohms, because the highest impedance seen by the driver will be actually around 85 ohms. With all the incremental impedance added, thereby achieving the lowest impedance, providing the necessary incremental impedance to get the overall impedance down to 20 ohms requires devices that are impractically large. Therefore, for the preferred embodiment the sizes were chosen so that resistances range from 32 ohms to 100 ohms in a nominal process.

As process conditions vary to the extremes, the device sizes chosen do not yield the same resistance values, but since this circuitry exploits feedback the matching scheme still works. In fact, the scheme has proven to work well under nominal test case conditions.

The target resistance values in the preferred embodiment of the present invention are as follows: (a) The main driver 100 ohms, (b) first increment 75 ohms, (c) second increment 200 ohms, (d) third increment 400 ohms.

These resistances provide output impedances in the range of 100 to 32 ohms, as shown in Table One (Fig. 4).

The following is a more detailed description of each of the elements of the driver shown in driver 3.

Figure 5 is a logic diagram of predriver 30 shown in Figure 3. The function of the predriver is to gate the driver enable signal with the driver input signal, while still allowing the output stage to provide a high impedance signal. This is accomplished by the utilization of NAND gate 70, inverter 72 and NOR gate 74, interconnected as shown. Predriver 30 ensures that: a) With logic input "1" only the pull-up devices are turned on, b) with logic input "0" only the pull-down devices are turned on, and c) in the high impedance state both the pull-up and pull-down devices are turned off, all of which is conventional for a so-called three-state driver.

Figure 6 shows the output stage 32 of Figure 3. The function of the output stage 32 is to provide current for the load. To optimize performance, the output stage 32 is used by the feedback circuitry (comparator 34, latches stage 36, and predriv r 30) to match the impedance to that of the load 40.

As described above, incremental impedanc components are provided as pairs of d vices, for

Fig. 7.

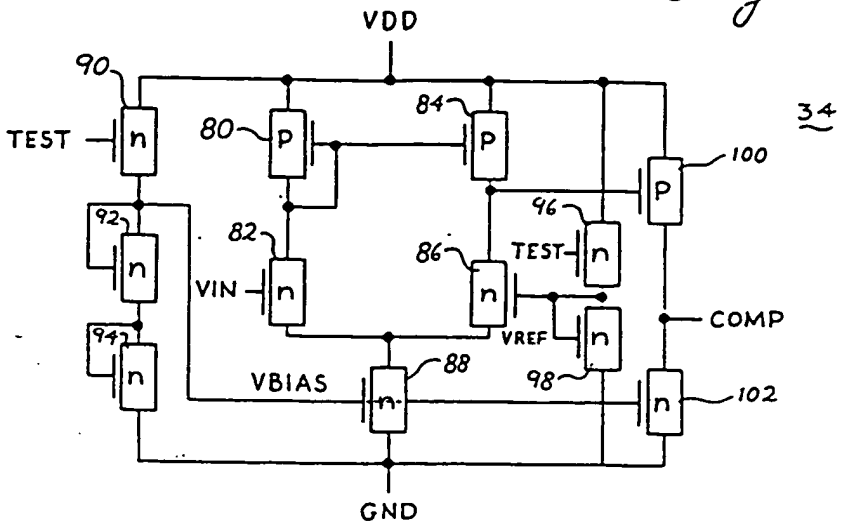

VDD
90
TEST
n
80
p
84
p
34
100
p
96
92
n
82
VIN
n
86
n
TEST
n
COMP
VREF
n
94
n
VBIAS
n
88
98
n
102
GND

Fig. 8A.

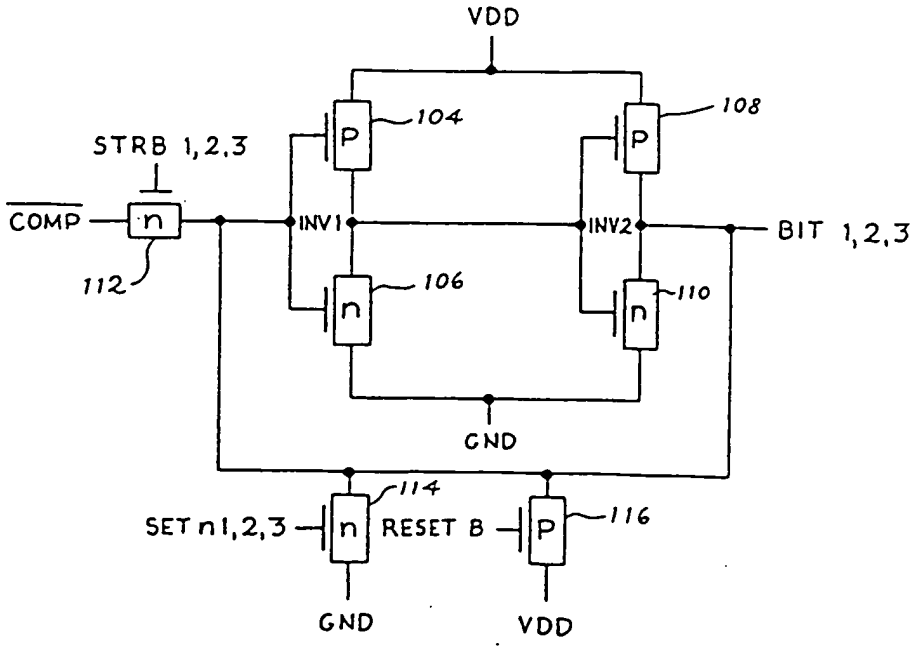
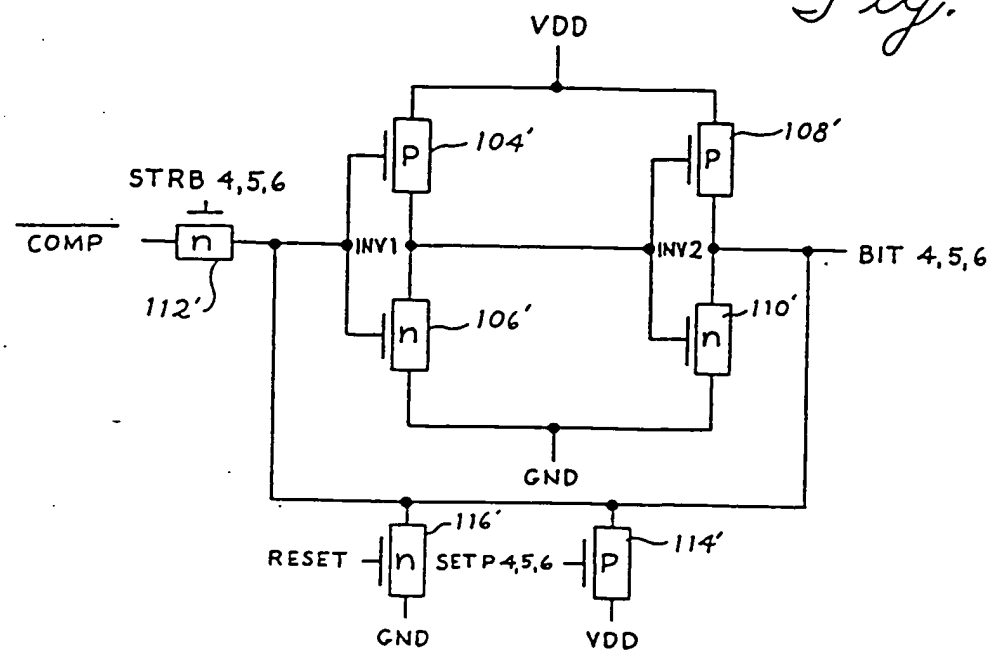

VDD
STRB 1,2,3
104
p
108
p
COMP
n
INV1
INV2
BIT 1,2,3
112
106
n
110
n
GND
114
SET n1,2,3
n
RESET B
p
116
GND
VDD

Fig. 8B.


VDD
P
104'
P
108'
STRB 4,5,6
COMP
n
112'
INV1
INV2
BIT 4,5,6
n
106'
n
110'
GND
116'
RESET
n
SETP 4,5,6
P
114'
GND
VDD

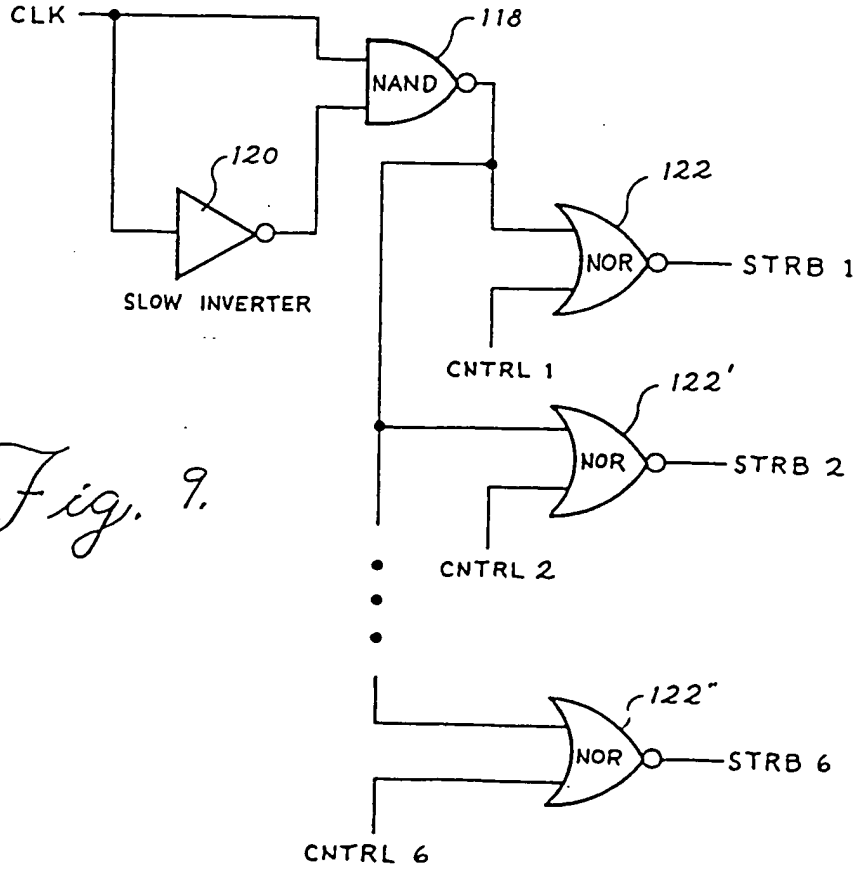

CLK
118
NAND
120
122
NOR
STRB 1
SLOW INVERTER
CNTRL 1
122'
NOR
STRB 2
CNTRL 2
122"
NOR
STRB 6
CNTRL 6

Fig. 9.

and a second combination of said second plurality of gat s and for enabling same.

Fig. 1. (PRIOR ART)

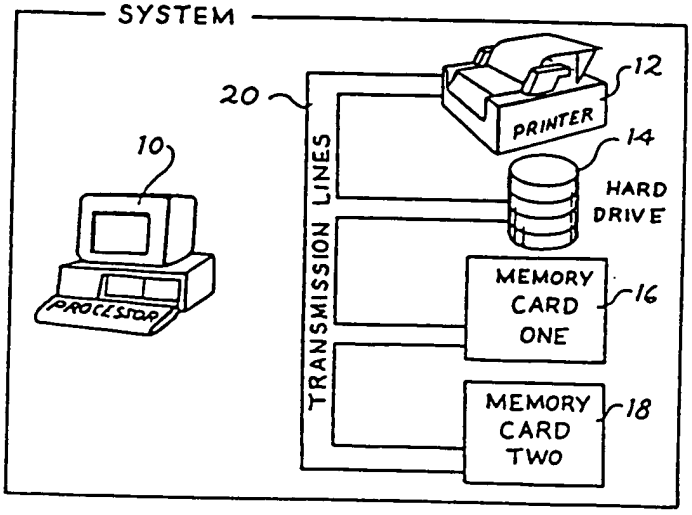
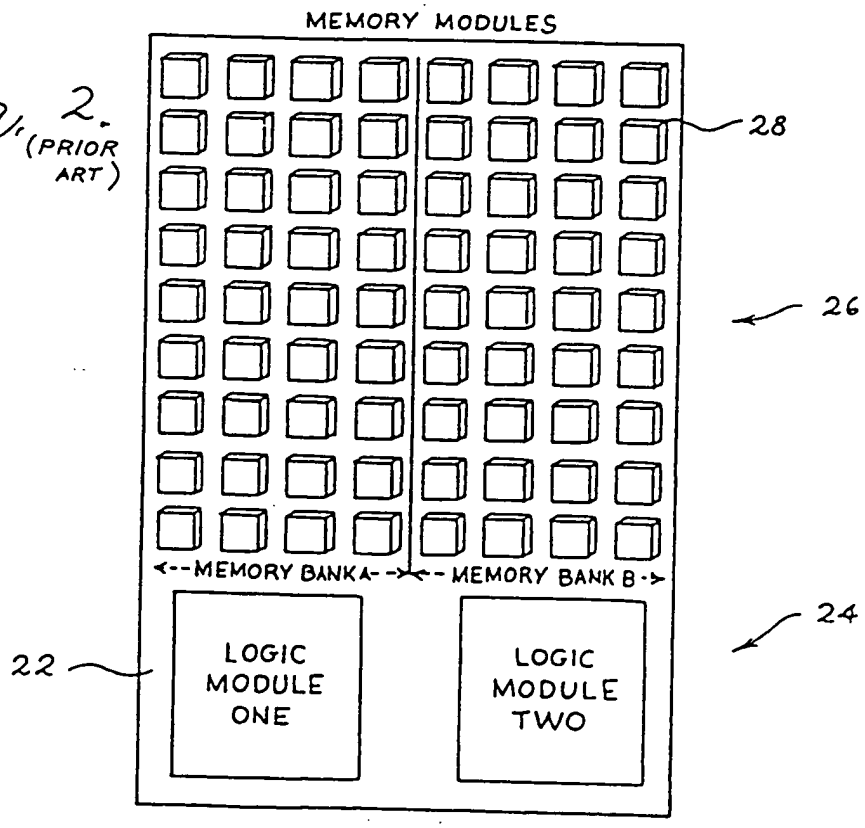


Fig. 2. (PRIOR ART)



example p-type devices 46 and 48, that are enabled to add their incremental impedance in parallel with the other driver output impedance to reduce the overall output impedance by a predetermined amount. The signal lines BIT1-6 control this enabling, and are provided from the latch circuits described below in connection with Figs. 8A and 8B.

Figure 7 is a circuit diagram of comparator 34 of Figure 3. Transistors 80, 82, 84, 86 and 88 comprise a conventional MOS differential amplifier. Devices 90, 92 and 94 comprise a voltage bias string that sets the bias for devices 88 and 102, device 90 also providing a switching function to turn the string on and off. The reference voltage, VREF, for the aforementioned comparison function is set by devices 96 and 98, also comprising a voltage bias string. Finally, devices 100 and 102 comprise an amplifier stage which, in addition to providing amplification also provides a level shift so that the output switches around a center at VDD/2. The output signal, COMP, is inverted and provided to the latches, as described below.

Figures 8A and 8B are circuit diagrams of the two kinds of latches employed in the set of latches 36 shown in Figure 3. Three sets each are used in set 36. The latch shown in Figure 8A, hereinafter referred to as latch 1, 2 or 3, as the case may be, is used to control the inclusion or omission of the device pairs 58-60, 62-64, and 66-68, respectively, shown in Figure 3, hereinafter designated as n-pair 1, 2 and 3. The latch shown in Figure 8B, hereinafter referred to as latch 4, 5 or 6, as the case may be, is used to control the inclusion or deletion of gate pairs 46-48, 50-52 and 54-56, respectively, shown in Figure 3, hereinafter referred to as p-pairs 4, 5 and 6.

Referring now to Figure 8A, devices 104, 106, 108 and 110 comprise a conventional latch, with devices 112, 114 and 116 providing strobe, set, and reset functions, respectively. The strobe signal applied to device 112, STRB1, 2 or 3, as the case may be, enables latching of the data signal "COMP," at the input of the latch. The circuit for generating the strobe signal is described below. The input signal is the inverted output signal from the comparator circuit described above in connection with Figure 7. Each of the latches 1, 2 and 3, having the configuration shown in Figure 8A gets, respectively, one of the signals SETN1, SETN2, or SETN3, as the case may be. These signals enable the strobing of the results of the comparator test to the latch, thus enabling the deletion of the associated gate pair from the output stage 32 in the sequence described above. The RESETB signal simply provides a reset function for the latch.

Figure 8B is a circuit diagram for latches 4, 5 and 6 of set 36. The operation of this latch circuit is substantially the same as that as the circuit described above in connection with Figure 8A. However, the polarities of the devices 114' and 116' are reversed from those of devices 114 and 116 of Figure 8A, to accommodate the different device polarities of device pairs 46-48, 50-52 and 54-56. Otherwise, operation of the circuit is the same.

Figure 9 is a block diagram of the timing circuits used to generate the aforementioned strobe signal from the system clock. The clock signal is applied to a first input of a NAND gate 118, and to a slow inverter 120, the output of which is connected to the second input of NAND gate 118. The circuit comprising manner gate 118 and slow inverter 120 is effectively a one shot circuit. The output of NAND gate 118 is provided to a first input of NOR gate 122 associated with latch 1, while a control signal from control logic 38 (Fig. 3) is provided to the second input thereof. The output of NOR gate 122 is the strobe signal for latch 1. It should be noted that in a given IC, the inverter 120 and NAND gate 118 are provided only once, with NOR gate 122 being provided in parallel for each latch in latch set 36, as shown by NOR gates 122', 122".

The operation of the control logic 38 in Figure 3 will now be described. Control logic 38 is comprised of conventional logic circuitry, the particular configuration of which is well within the design skills of one of ordinary skill in this art. The particular circuit configuration is not particularly pertinent, the significant aspect of control logic 38 being the timing of the various signals produced thereby and applied to the other parts of the circuit shown in Figure 3. It should be noted that in adapting the preferred embodiment to its design system, the control logic 38 is provided only once for a given IC circuit, the remainder of the driver circuitry being provided with each driver throughout the IC circuit.

The control logic 38 sends out test voltage pulses, and when the impedance matching is complete turns the feedback circuity off. Control logic 38 carries out the sequence of tests involved in impedance matching the output stage 32 to the load, as described above. The control logic 38 is the interface between the digital data system (not shown) and the driver, and is intended to be transparent to the system, except that the system, after powering up, sends a signal to the control logic 38 causing the control logic 38 to initiate the test sequence, after which the control logic sends a signal to the system indicating that set-up is complete.

Referring now to Figure 10, initially the Enable signal is activated to allow the predriver 30 (Fig. 3) to send data signals to the output stage 32, rather than remain in a high impedance state. At the

Fig. 5.

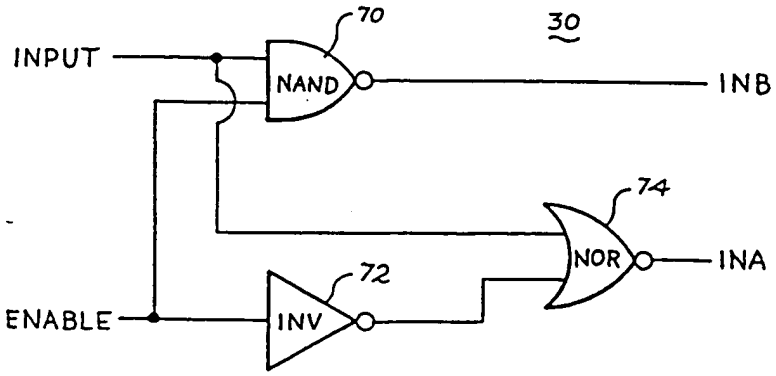

INPUT
NAND
70
30
INB
74
NOR
INA
72
INV
ENABLE

Fig. 6.

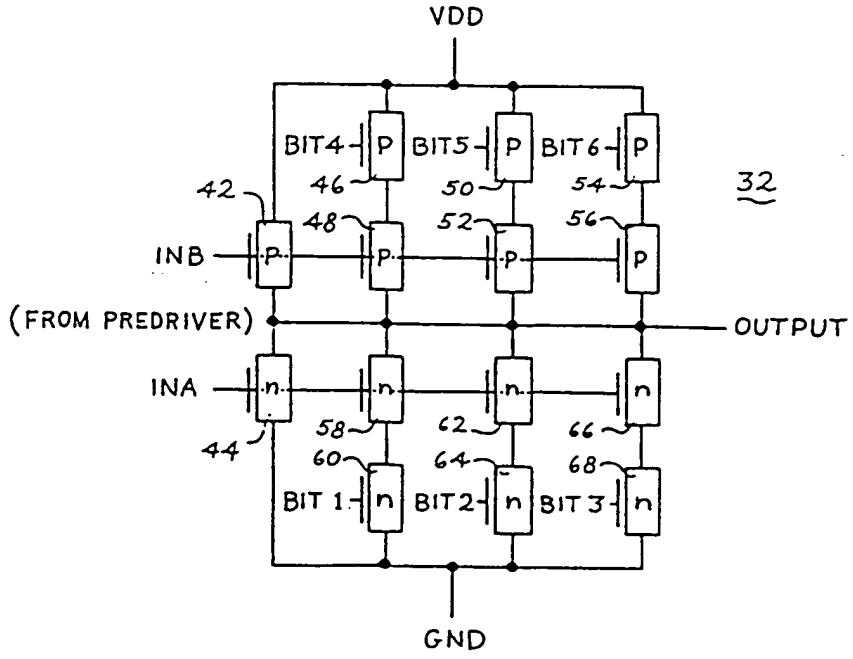
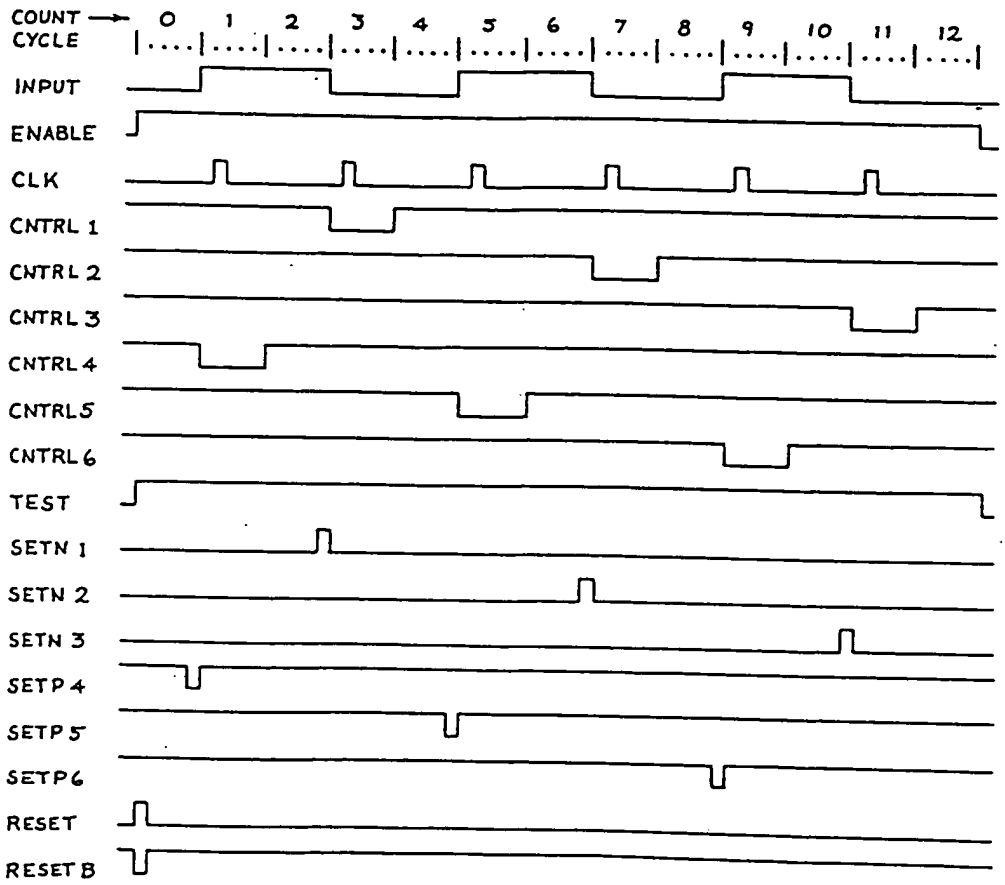

VDD
BIT4
P
BIT5
P
BIT6
P
46
50
54
42
48
52
56
32
INB
P
P
P
P
(FROM PREDRIVER)
OUTPUT
INA
n
n
n
n
58
62
66
44
60
64
68
BIT 1
n
BIT2
n
BIT 3
n
GND

Fig. 10.


COUNT
CYCLE
0
1
2
3
4
5
6
7
8
9
10
11
12
INPUT
ENABLE
CLK
CNTRL 1
CNTRL 2
CNTRL 3
CNTRL 4
CNTRL 5
CNTRL 6
TEST
SETN 1
SETN 2
SETN 3
SETP 4
SETP 5
SETP 6
RESET
RESET B

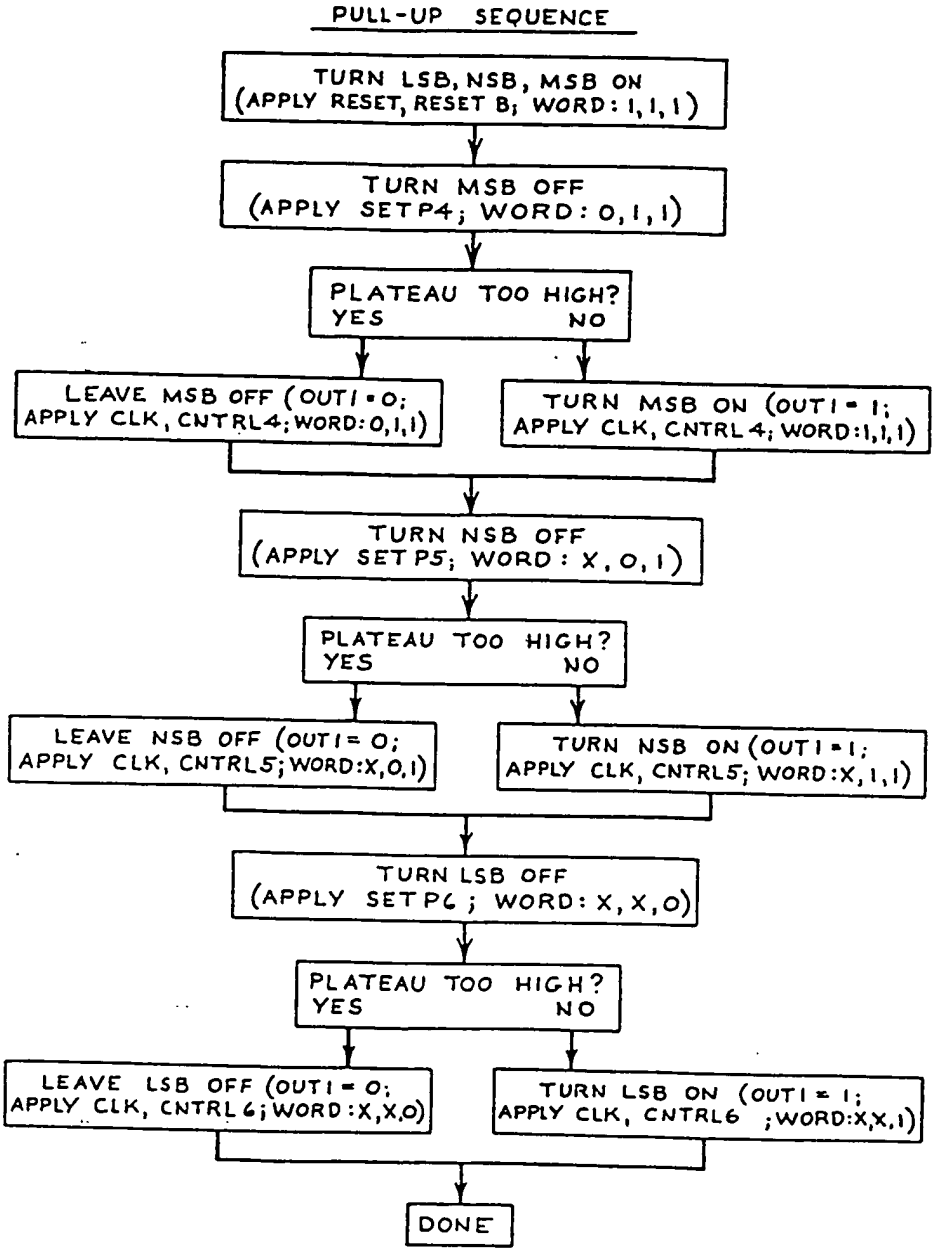

PULL-UP SEQUENCE
TURN LSB, NSB, MSB ON (APPLY RESET, RESET B; WORD: 1,1,1)
TURN MSB OFF (APPLY SETP4; WORD: 0,1,1)
PLATEAU TOO HIGH? YES NO
LEAVE MSB OFF (OUT1 = 0; APPLY CLK, CNTRL4; WORD: 0,1,1)
TURN MSB ON (OUT1 = 1; APPLY CLK, CNTRL4; WORD: 1,1,1)
TURN NSB OFF (APPLY SETP5; WORD: X, 0, 1)
PLATEAU TOO HIGH? YES NO
LEAVE NSB OFF (OUT1 = 0; APPLY CLK, CNTRL5; WORD: X,0,1)
TURN NSB ON (OUT1 = 1; APPLY CLK, CNTRL5; WORD: X, 1, 1)
TURN LSB OFF (APPLY SETP6; WORD: X, X, 0)
PLATEAU TOO HIGH? YES NO
LEAVE LSB OFF (OUT1 = 0; APPLY CLK, CNTRL6; WORD: X,X,0)
TURN LSB ON (OUT1 = 1; APPLY CLK, CNTRL6; WORD: X,X,1)
DONE

Fig. 11A.

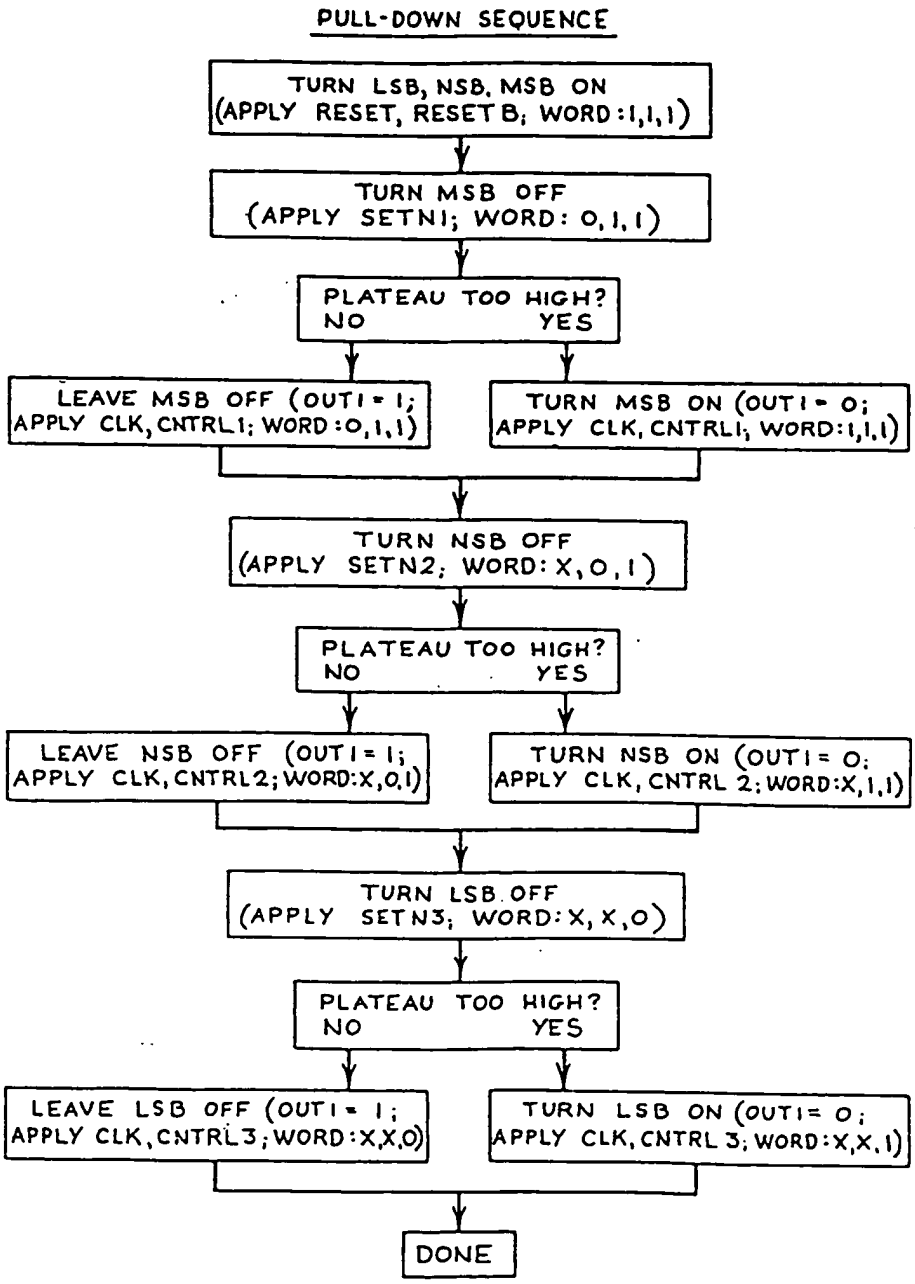

PULL-DOWN SEQUENCE
TURN LSB, NSB, MSB ON (APPLY RESET, RESET B; WORD:1,1,1)
TURN MSB OFF (APPLY SETN1; WORD: 0,1,1)
PLATEAU TOO HIGH? NO YES
LEAVE MSB OFF (OUT1 = 1; APPLY CLK, CNTRL1; WORD:0,1,1)
TURN MSB ON (OUT1 = 0; APPLY CLK, CNTRL1; WORD:1,1,1)
TURN NSB OFF (APPLY SETN2; WORD: X,0,1)
PLATEAU TOO HIGH? NO YES
LEAVE NSB OFF (OUT1 = 1; APPLY CLK, CNTRL2; WORD:X,0,1)
TURN NSB ON (OUT1 = 0; APPLY CLK, CNTRL 2; WORD:X,1,1)
TURN LSB OFF (APPLY SETN3; WORD: X, X, 0)
PLATEAU TOO HIGH? NO YES
LEAVE LSB OFF (OUT1 = 1; APPLY CLK, CNTRL3; WORD:X,X,0)
TURN LSB ON (OUT1 = 0; APPLY CLK, CNTRL 3; WORD:X,X,1)
DONE

Fig. 11B.

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91106666.0

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US - A - 4 912 724 (WILSON) * Column 1, line 26 - column 2, line 2; column 2, line 52 - column 4, line 26; fig. 1-3 * --	1,2	H 04 L 12/40 H 04 B 3/36 H 04 B 3/50 G 06 F 13/36
A	DE - B2 - 2 537 383 (LICENTIA) * Claims 1,2; column 1, line 28 - column 2, line 52; fig. 1 * --	1,2	
A	EP - A2 - 0 364 700 (ANT NACHRICHTENTECHNIK) --		
A	EP - A2 - 0 323 586 (GTE LABORATORIES) ----		

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 04 L
H 04 B
G 06 F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	03-10-1991	HAJOS

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)

same time the Test signal is applied, which powers up the comparator 34. Following this, the RESET and RESETB signals are pulsed, causing the latches 36 to be s t in a state which causes all the incremental impedance gate pairs in the output stage 32 to be enabled.

Then the SETP4 line is pulsed, setting the latch associated with the most significant bit of p-chann l impedance, latch 4, removing it from the output stage 32.

Next, a positive going input pulse is applied to the Input line of the predriver 30. Shortly thereafter the CNRTL4 line is brought low, and the CLK signal is pulsed, capturing the results of the comparator 34 comparison in the latch associated with bit 4, allowing for propagation delays and settling of the output signal, the timing of this being determined by the CLK signal.

The SETN1 signal is then pulsed, turning off the most significant bit of n-channel impedance, followed by the negative going transition of the Input signal, the CNTRL1 signal, and the CLK signal, as above, capturing the results of the test in the latch associated with bit 1.

The sequence continues, alternating between p-channel and n-channel test, testing with respect to the next significant bit, and finally, the least significant bit, completing the test.

Figure 11A is a flow chart illustrating the above-described sequence in terms of logic flow, and connecting the logic flow to the sequence of signals, for the pull-up incremental impedance pairs. Figure 11B is a flow chart like that of Figure 11A, but for the pull-down pairs. In implementation, these charts are, in effect, "interleaved," as the test proceeds alternatingly on "rising" transitions and "falling" transitions of the input signal, adjusting alternatingly the pull-up pairs and then the pull-down pairs, incrementally.

In Figures 11A and 11B, reference is made to "word." This word corresponds to the three bits of incremental impedance, indicating whether a particular incremental impedance pair in "ON" (bit "1") or "OFF" (bit "0"). A value of "X" indicates that in that branch of the flow chart, such bit has whatever value was set for that bit position in the previous operation or operations. Thus, a word value of 1, 0, 1 corresponds to a condition where the most and least significant bit are "ON," while the "next" significant bit is "OFF." Also, a word value of 1, X, 0 corresponds to a condition where the most significant bit is "ON," the least significant bit is "OFF," and the next significant bit is whatever value it was set in the previous operation or operations. R fer to Tabl 1 (Fig. 4) for the next output impedance valu any particular word value represents.

Claims

1. A self-adjusting impedance matching driver for a digital circuit, driving a load having an unknown impedanc within a pr determined range, comprising:

   driver means (32) for driving digital signals to a digital circuit, said driver means having a predetermined impedance;

   said driver means including selectable impedance means for changing said predetermined impedance to a different, selected impedance within said predetermined range; and

   means (34, 36, 38) coupled to said driver means for sensing the impedance difference between the output of said driver means and the digital circuit and for modifying automatically said selectable impedance means to a different impedance to obtain the optimum impedance match of said driver means to the digital circuit.

2. The self-adjusting impedance matching driver of claim 1, wherein said driver means comprise a driver amplifier connected to a driver input, comprising a pull-up amplifier connected to the supply voltage source and a pull-down amplifier connected to the circuit ground.

3. The self-adjusting impedance matching driver of claim 2, wherein a first plurality of gates is connected in parallel between he output of said driver amplifier and the supply voltage source.

4. The self-adjusting impedance matching driver of claim 3, wherein a second plurality of gates connected in parallel between the output of said driver amplifier and the circuit ground.

5. The self-adjusting impedance matching driver of claim 1 to 3, wherein said selectable impedance means selectively enable any combination of said first plurality of gates and, independently, any combination of said second plurality of gates, such that any of a plurality of impedances may be selected for the output of said driver, independently for both the pull-up and pull-down transitions of said driver amplifier.

6. The s lf-adjusting impedance matching driver of claim 5, wherein said impedance differenc sensing means for automatically s lecting a first combination of said first plurality of gat s

transistors, and for enabling the same. Th first and second combinations are s lected to provide the optimum impedance match to th particular impedance of the load.

Th application of the principles of the pres nt invention is advantageous in configurable systems because the impedance of driv r loads can vary greatly from configuration to configuration. Application of the principles disclosed herein improve the noise, overshoot and undershoot problems by matching the load. Further advantages are obtained because the present invention automatically adjusts the output impedance of the driver to the impedance of the circuit that it drives.

The foregoing and other objects, features, aspects and advantages of the invention will be apparent from the following more particular description of the preferred embodiments of the invention, as illustrated in the accompanying drawings, in which:

Figure 1
shows a prior art computer processor system configuration;

Figure 2
shows a prior art memory card including two memory module banks, each being driven by a logic module;

Figure 3
is a block diagram of a preferred embodiment of the present invention;

Figure 4
is a table showing combinations and corresponding output impedance values for various selections of the transistors shown in Figure 3;

Figure 5
is a logic diagram of the predriver stage shown in Figure 3;

Figure 6
is a circuit diagram of the output stage of the driver shown in Figure 3;

Figure 7
is a circuit diagram of the comparator shown in Figure 3;

Figs. 8A and 8B
are circuit diagrams of two latch circuits employed in the set of latches 36 shown in Figure 3;

Figure 9
is a circuit diagram of a timing generation circuit used in the embodiment shown in Figure 3;

Figure 10
is a diagram showing control circuitry critical timing for the implementation depicted in Figure 3; and

Figs. 11A and 11B
are flow chart diagrams illustrating the sequence of events for pull-up pairs and pull-down pairs of gates, respectively.

Figure 3 is a block diagram of the preferred mbodiment of the pres nt invention. The basic components are a predriver 30 an output stage 32 a comparator 34, a set of latches 36 and a control logic block 38. The utput of th output stage 32 drives a load 40 which, in gen ral, has a fixed, but unknown impedance within a known range.

The output stage 32 comprises an array of p-type and n-type MOS transistors, the preferred embodiment being implemented in CMOS technology. The primary driver devices are p-type device 42 and n-type device 44. Device 42 is a pull-up transistor, while device 44 is a pull-down transistor. VDD is the circuit supply voltage, GND being circuit ground. Also included in output stage 32 are three pairs of p-type devices 46-48, 50-52 and 54-56, connected between the output line and VDD. Devices 48, 52 and 56 are gated by the output of predriver 30, while devices 46, 50 and 54 are gated independently by the outputs of the set of latches 36. Likewise, three pairs of n-type devices 58-60, 62-64 and 66-68 are provided between the output line and ground, the operation thereof being similar to that of the three pairs of p-type devices just described.

The primary driver devices 42, 44 have a characteristic impedance equal to the highest anticipated impedance to be presented under normal conditions by load 40. Each of the pairs of devices just described has a preselected characteristic impedance which, when added in parallel to the impedance of devices 42 and 44, as the case may be, serves to reduce the characteristic impedance of the output stage 32 in a selectable manner. The addition or omission of the pairs of devices just described, referred to herein as "incremental impedance pairs," or "incremental impedance devices," is controlled by the operation of the set of latches 36 under control of the control logic 38, in a manner which is described below.

In a test iteration, an input signal and an enable signal are applied to the predriver 30 causing an output signal to appear on the output of output stage 32. Sufficient time is allowed for the enabled input signal to propagate through the drive circuitry, and for any transient components to substantially subside at the output. The output signal is then considered to be at a "plateau". This output signal plateau voltage is applied to comparator 34 where it is compared against a reference voltage. When the impedance of output stage 32 and the impedance of load 40 are substantially the same, representing a balanced impedance condition, the voltage appearing at the output of output stage 32 is substantially one half of VDD. Thus, the reference voltage is set at VDD/2.

The test sequence continues through several tests in which the aforementioned voltage compari-